ABSTRACT

A sample hold circuit (14) includes a first switch (15) connected between a data line (6) and a first node (N10), a second switch (16) connected between first node (N10) and a second node (N20), a capacitor (19) connected between the second node (N20) and a line of a common potential (VCOM), and a drive circuit (20) applying a potential equal to that of the second node (N20) to the first node (N10) and one of the electrodes of the liquid crystal cell (2). The first and second switches (15 and 16) are turned on when a scanning line (4) is at an "H" level.